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Supplementary information

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A 64-kilobit spin–orbit torque magnetic random-access memory based on back-end-of-line-compatible β-tungsten

In the format provided by the authors and unedited

Supplemental Information

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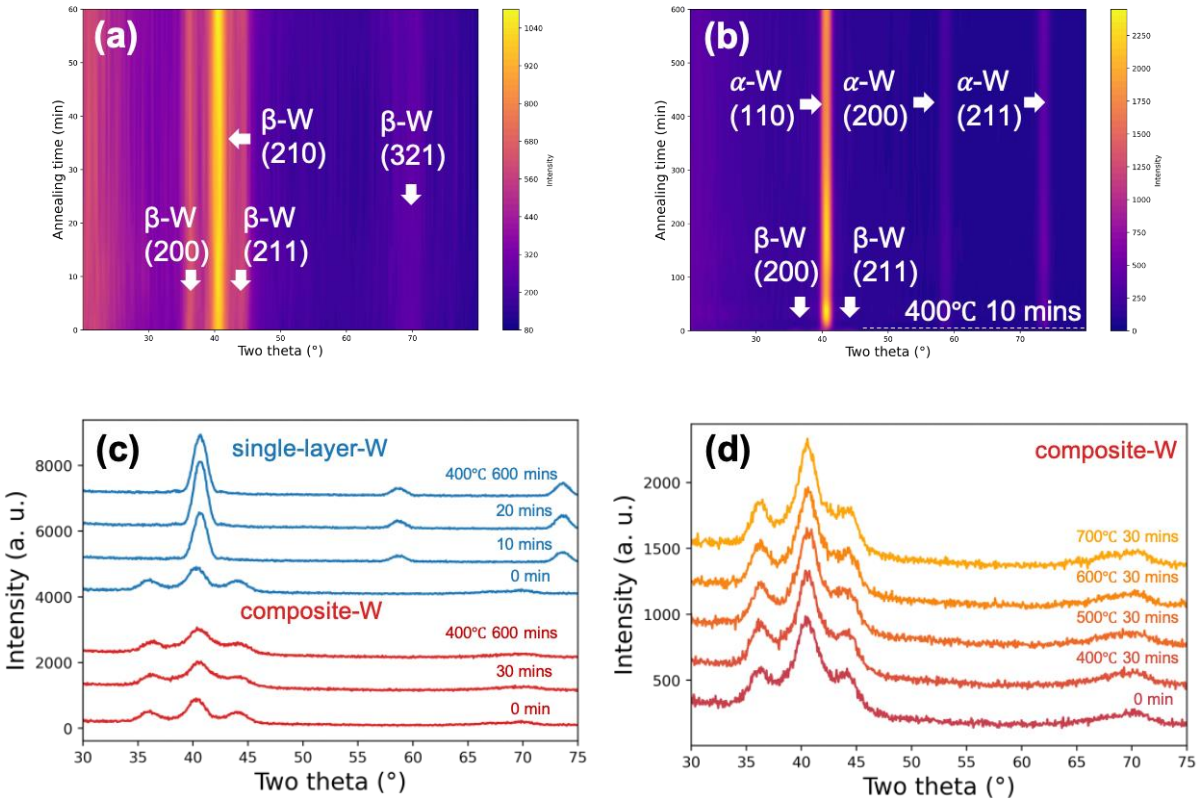
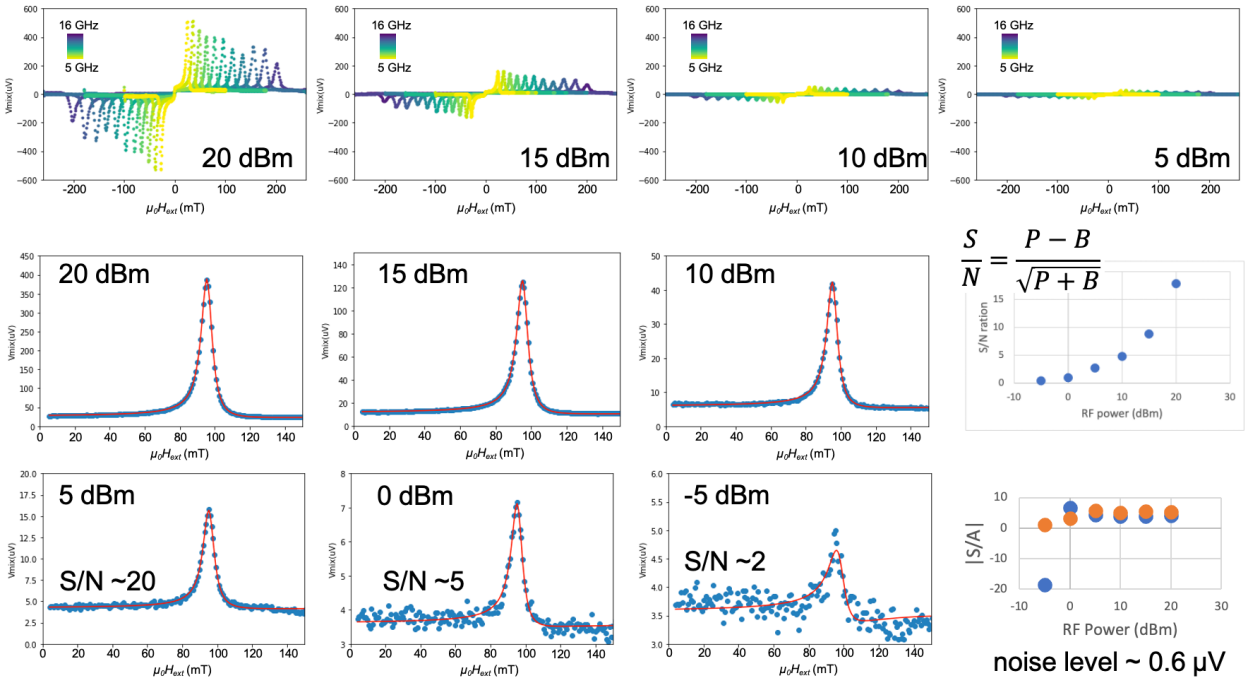
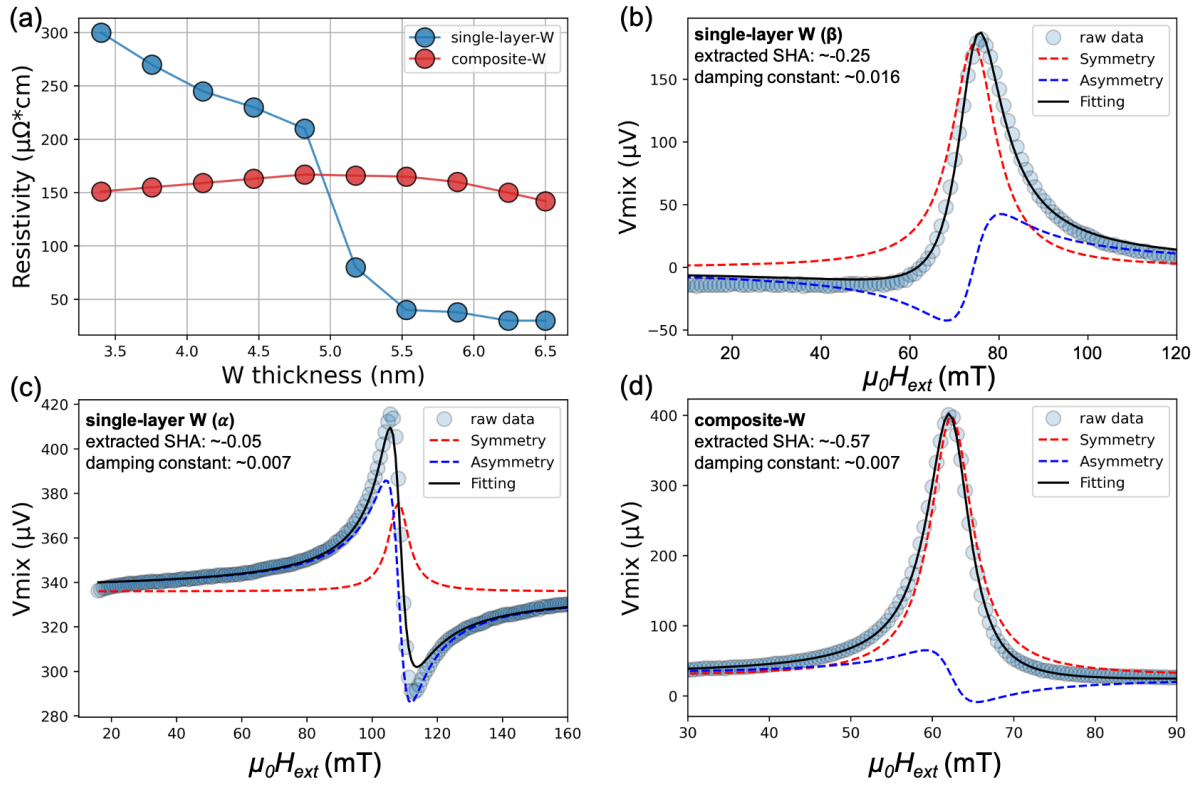


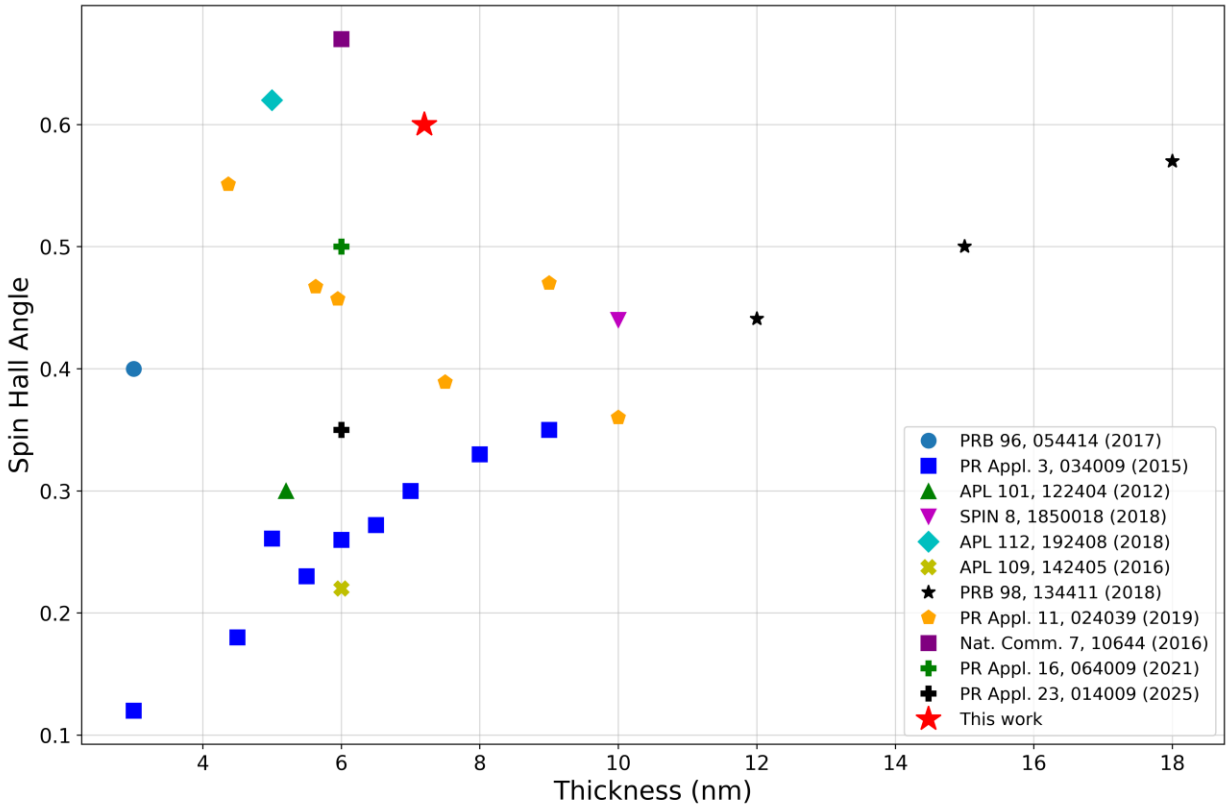
S1. Gracing incident X-ray diffraction patterns of single-layer-W and composite-W samples. (a) Contour plot of GIXRD patterns demonstrating the robust thermal stability of 6.6-nm composite-W, which retains the β-phase even after 10 hours of annealing at 400°C. Peaks corresponding to β-W (200), β-W (210), β-W (211), and β-W (321) are indicated. (b) Contour plot showing the phase transformation of 6.5-nm single-layer W, where α-W peaks emerge after just 10 minutes of annealing at 400°C, indicating a transition from the β-phase. (c) Time-dependent GIXRD patterns of single-layer W (blue) and composite-W (red) under 400°C annealing for various durations, demonstrating the gradual phase transformation. (d) Temperature-dependent GIXRD patterns of composite-W annealed at different temperatures for 30 minutes, revealing the thermal stability and phase evolution.



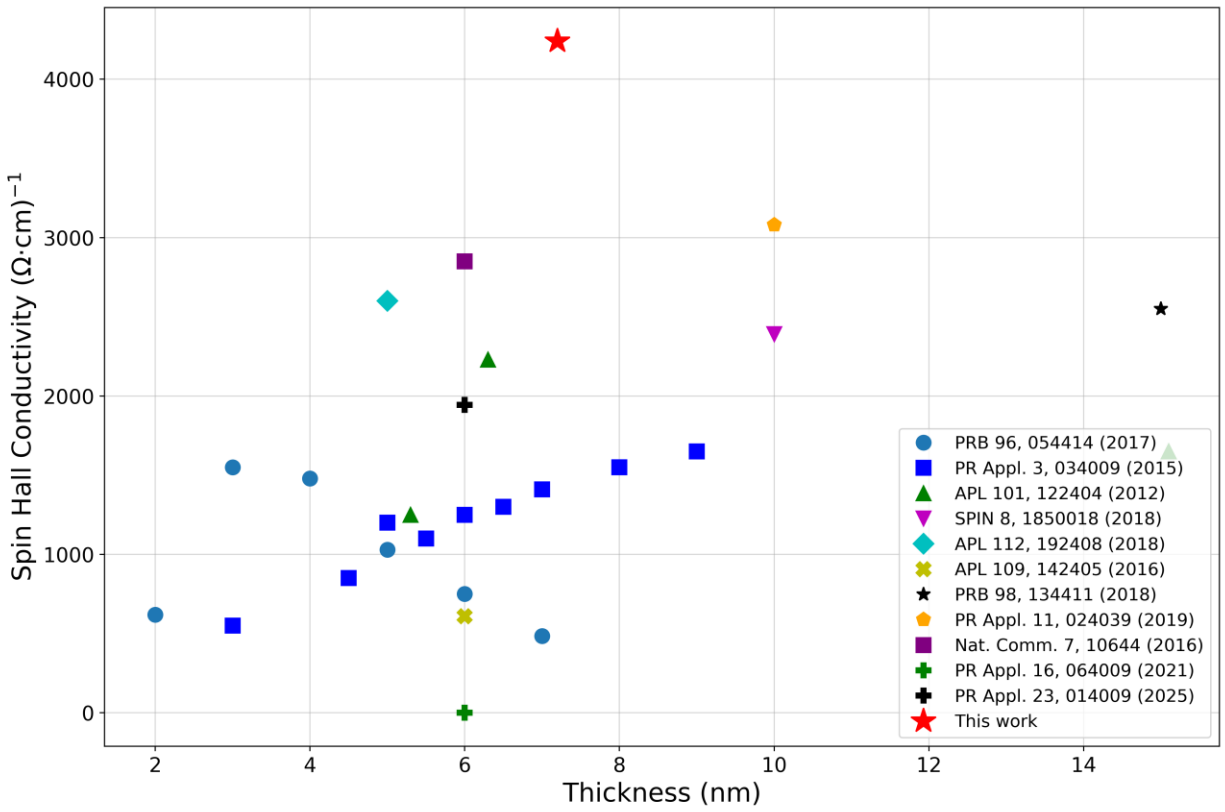
S2. Power dependence on ST-FMR spectrum.



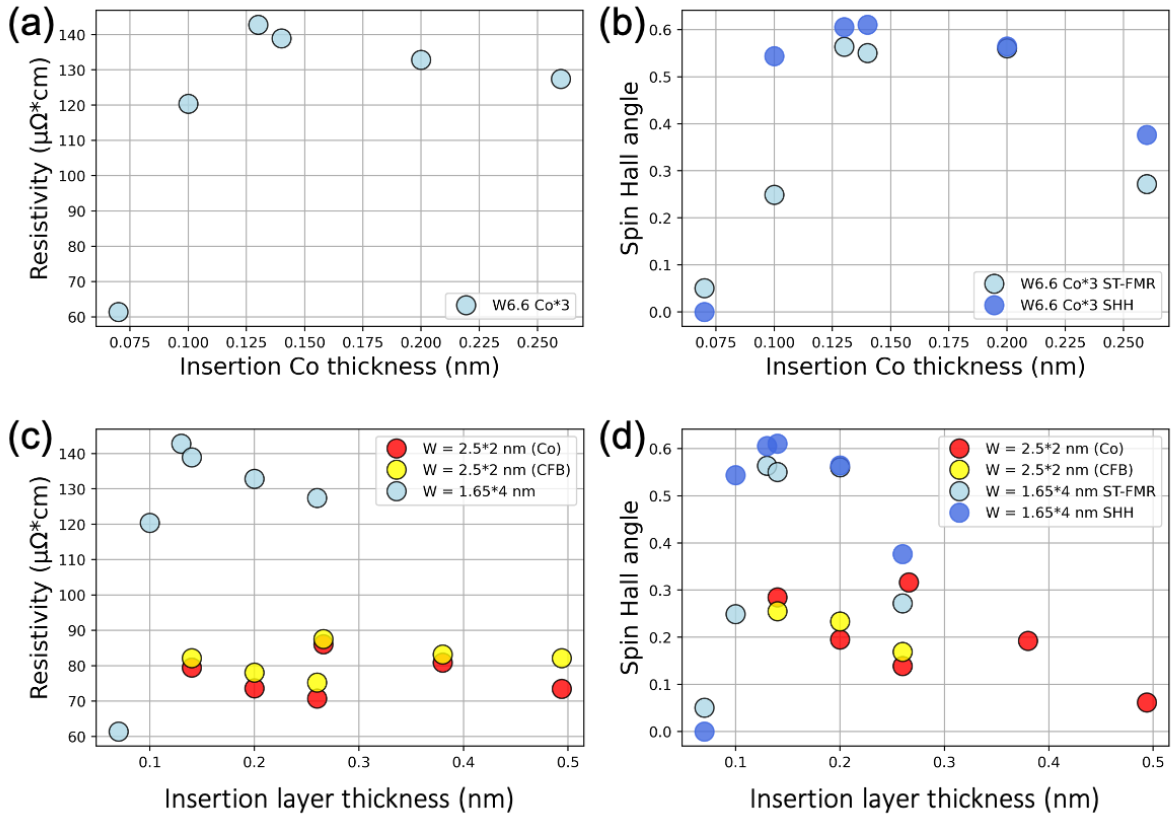
S3 Phase transformation from β-W to α-W and corresponding ST-FMR Spectra. (a) Thickness dependence of composite-W (red) and single-layer W (blue) after 30 min of annealing at 400 °C, showing that the β-phase in single-layer W remains stabilised only below ~5 nm. (b) ST-FMR spectrum of a 6.5-nm single-layer W sample without the 1 T 400 °C for 30 min magnetic annealing, yielding an extracted spin Hall angle of ~−0.25. In the absence of magnetic annealing, the tungsten/free-layer interface degrades, increasing the damping constant and compromising spin Hall angle. (c) ST-FMR spectrum of the same 6.5-nm single-layer W after the 1 T 400 °C for 30 min magnetic annealing. Although the damping constant is significantly improved, the spin Hall angle decreases to about −0.05, reflecting the conversion of β-W to α-W. (d) The typical ST-FMR spectrum for 6.6-nm composite-W after the magnetic annealing process.



S4. Spin Hall angle benchmarking. Remade from PR Appl. 4, 094404 (2020) ref. [1]. Spin Hall angle benchmarking of tungsten-based heterostructures. The plot compares values of spin Hall angle reported in literature for various W-based systems. All data shown correspond to β-phase tungsten (β-W), except for ref. 6 and 9 which do not specify the W-phase, and ref. 7, which reports on nanocrystalline W. The red star represents the result from this work. Data sources: PRB 96, 054414 (2017) (ref. [2]); PR Appl. 3, 034009 (2015) (ref. [3]); APL 101, 122404 (2012) (ref. [4]); SPIN 8, 1850018 (2018) (ref. [5]); APL 112, 192408 (2018) (ref. [6]); APL, 109, 142405 (2016) (ref. [7]); PRB, 98, 134411 (2018) (ref. [8]); PR Appl. 11, 024039 (2019) (ref. [9]); Nat. Commun. 7, 10644 (2016) (ref. [10]); PR Appl. 16, 064009 (2021) (ref. [11]); PR Appl. 23, 014009 (2025) (ref. [12]); and this work.

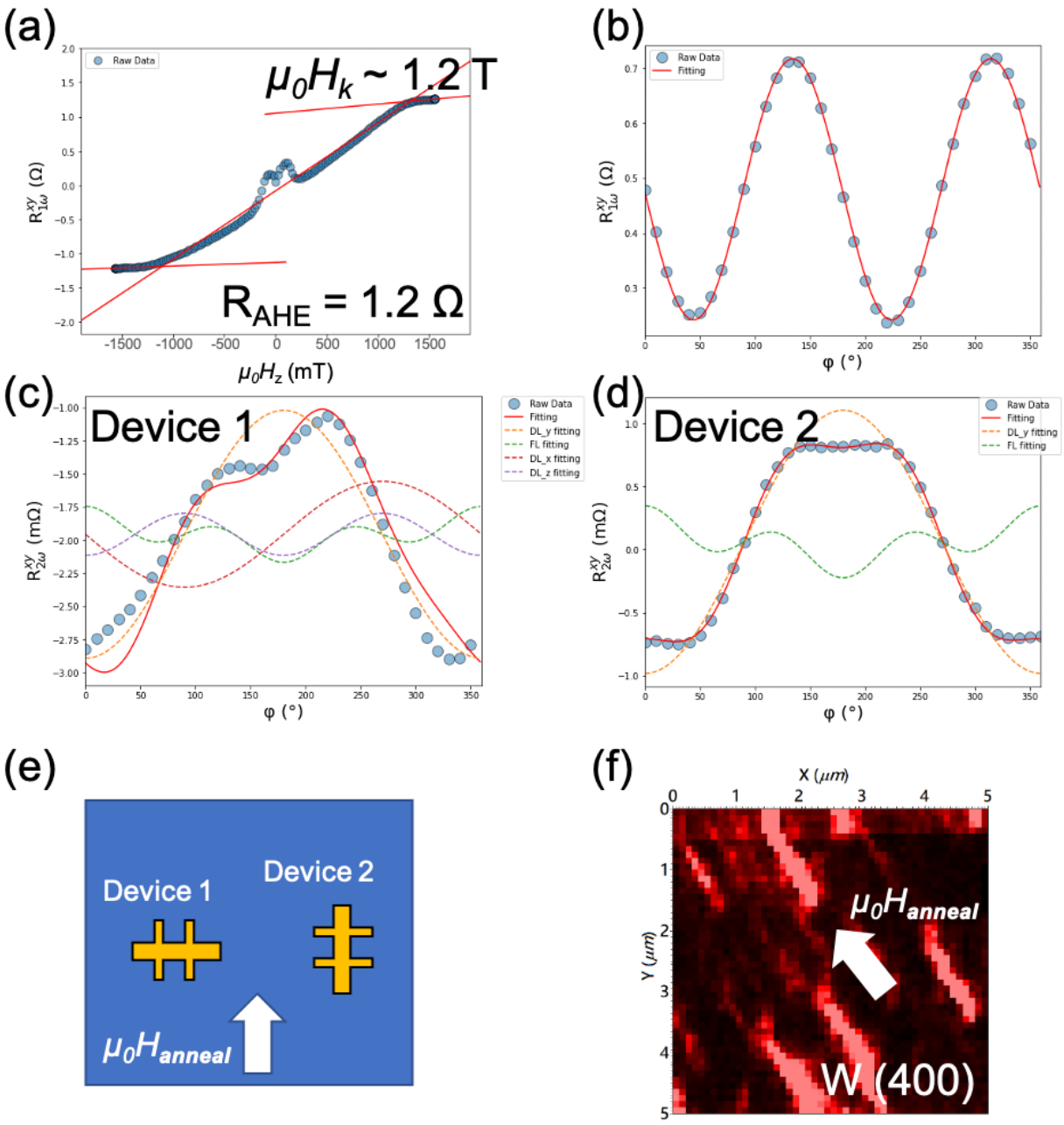


S5. Spin Hall conductivity benchmarking. Remade from PR Appl. 4, 094404 (2020) ref. [1]. Spin Hall conductivity benchmarking of tungsten-based heterostructures. The plot compares values of spin Hall angle reported in literature for various W-based systems. All data shown correspond to β-phase tungsten (β-W), except for ref. 6 and 9 which do not specify the W-phase, and ref. 7, which reports on nanocrystalline W. The red star represents the result from this work. Data sources: PRB 96, 054414 (2017) (ref. [2]); PR Appl. 3, 034009 (2015) (ref. [3]); APL 101, 122404 (2012) (ref. [4]); SPIN 8, 1850018 (2018) (ref. [5]); APL 112, 192408 (2018) (ref. [6]); APL, 109, 142405 (2016) (ref. [7]); PRB, 98, 134411 (2018) (ref. [8]); PR Appl. 11, 024039 (2019) (ref. [9]); Nat. Commun. 7, 10644 (2016) (ref. [10]); PR Appl. 16, 064009 (2021) (ref. [11]); PR Appl. 23, 014009 (2025) (ref. [12]); and this work.



S6. Resistivity and spin Hall angle as a function of the Co/CFB insertion layer thickness. (a) Dependence of resistivity on Co insertion layer thickness for composite-W, the same tested structures shown in Figure 2 in the main text. (b) Dependence of Spin Hall angle on insertion layer thickness for composite-W, the same tested structures shown in Figure 2 in the main text. (c) Dependence of resistivity on insertion layer thickness for W sub-layers of 2.5 nm, with Co and CoFeB (CFB) insertion layers represented by red and yellow dots, respectively. (d) Dependence of Spin Hall angle on insertion layer thickness for W sub-layers of 2.5 nm, with Co and CoFeB (CFB) insertion layers represented by red and yellow dots, respectively. The blue data points are referring to the tested structures shown in Figure 2 in the main text.

Note 1. Unconventional spin in composite-W sample.



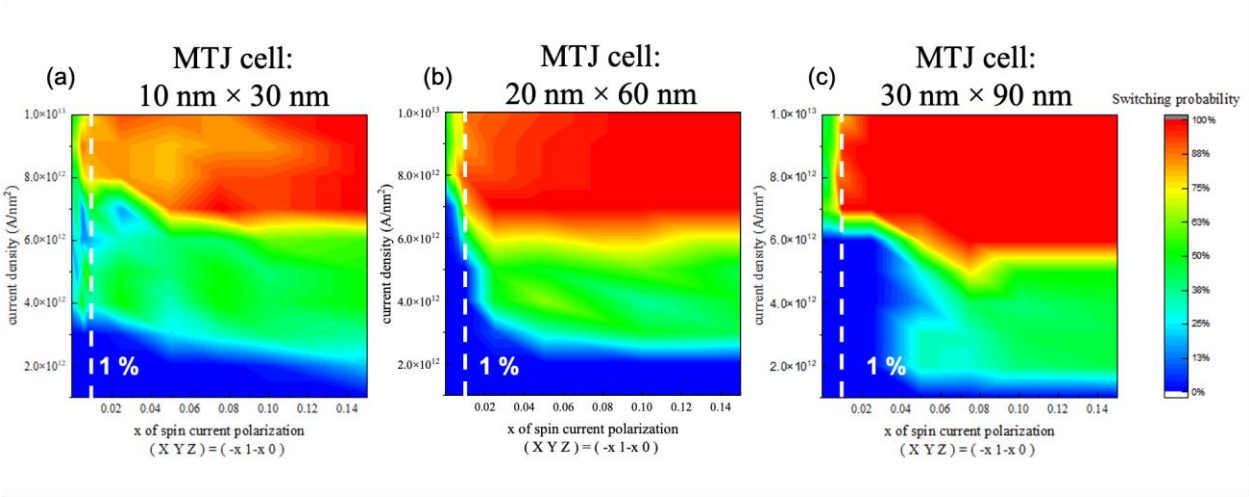
S7. Harmonic Hall measurements of SOTs in the composite-W structures. a, Typical first harmonic Hall resistance under out-of-plane external field. b, Typical angular dependence of first harmonic Hall resistance. **c** and **d**, the second harmonic Hall resistance measured from two different device geometry shown in **e**. Device 1 has current channel perpendicular to the field annealing direction, and device 2 has the current passing parallel to the field annealing direction. **f**, The composite-W texture revealed by nano-X-ray diffraction mapping.

$$R_{H,2\omega} = R_{AD,x}\sin\varphi + R_{AD,y}\cos\varphi + R_{AD,z}\cos 2\varphi + R_{FL,x}\cos 2\varphi\sin\varphi + R_{FL,y}\cos 2\varphi\cos\varphi + R_{FL,z}$$

S7 illustrates the two devices we study here, in device 1(2), the current is running perpendicularly (parallelly) to the magnetic field annealing direction. **S7c** and **d** show the $\emptyset$ dependence of $R_{1\omega}^{xy}$ and $R_{2\omega}^{xy}$ of device 1 fabricated on the 6.6-nm composite W sample, respectively, under H_{ext} = 0.155 T. We can obtain the R_P of device 1 is 237 mΩ by the fitting result shown in **S7c**. The representative measured $R_{2\omega}^{xy}$ (open circles) is plotted in **S7d** and fitted with the corresponding equation above (dash lines). We can learn that the data is well fitted with mainly H_{DL}^{y} term, which has $cos\,\emptyset$ dependence, and partially with H_{DL}^{x}, H_{DL}^{z}, and H_{FL}^{y}. To quantitively extract the magnitude of these terms, we conducted H_{ext} dependence measurements ranging from 277 Oe to 2100 Oe (preventing the non-linear response at the small field). **S7d** shows the overall fitting results that clearly exhibit asymmetric behavior (non-$cos\,\emptyset$ dependence). This implies the device 1 in our sample can generate a non-convectional spin polarisation, which can trigger field-free switching of Type-X(Z) SOT-MRAM. On the other hand, we carried out the same measurements on device 2, in which we have R_P = 244 mΩ, and symmetric $R_{2\omega}^{xy}$ behavior ($cos\,\emptyset$ dependence) as shown in **S7d**. From the field dependence data, we can extract all the fitted terms and calculate the damping(field)-like torque efficiency originated from three components by $\xi_{DL}^{i} = \frac{2e}{\hbar}\frac{H_{DL}M_S t}{j_{W-Co}}$ and $\xi_{FL}^{i} = \frac{2e}{\hbar}\frac{H_{FL}M_S t}{j_{W-Co}}$ summarised in **table S1**, where i = x, y, or z, and j_{W-Co} is the current density running through the W-Co layer.

Table S1. Summary table for all the terms extracted from 2nd harmonic Hall resistance measurements.

	ξ_{DL}^{y}	$\mu_0 H_k$ (T)	$I_0 \alpha \nabla T$ (Oe)	ξ_{FL}^{y}	ξ_{DL}^{x}	ξ_{DL}^{z}	ξ_{FL}^{x}	θ_{SH} by ST-FMR
Device 1	0.65	1.1	1	~0	0.006	~0	~0	0.52
Device 2	0.51	1.1	1	~0	~0	~0	~0	0.52



S8. Micromagnetic simulations of switching probability for unconventional SOT switching for elliptical magnetic tunnel junctions of different lateral sizes: (a) 10 nm × 30 nm, (b)

20 nm × 60 nm, and (c) 30 nm × 90 nm. The spin polarization vector is defined as (X, Y, Z) = (−x, 1−x, 0), where x represents the contribution of the unconventional in-plane spin component. Simulations show that even a 1% x-component (indicated by the white dashed line) is sufficient to induce deterministic field-free switching in Type-X geometry at sufficiently high current densities. These results highlight the critical role of unconventional spin textures in enabling low-field or field-free spin–orbit torque (SOT) switching.

Field-free spin–orbit torque switching

To explore the possibility of using ξ_{DL}^{x} to achieve field-free Type-X SOT switching, we firstly model our system by micromagnetic simulation in oommf (Object-Oriented MicroMagnetic Framework) software for switching study[13]. In our model, we set a free-layer in three different sizes – from 30-10 nm by 90-30 nm by 1 nm elliptical disk with in-plane anisotropy along x-direction (as shown in **S8**) with spin polarisation vector [-x,1-x,0], where 1 represents 100% conventional spin polarisation. From the simulations shown in **S8**, we can find that 1% of x-component is sufficient to realise the type-x field-free switching at the high current density region. We have also demonstrated the type-x field-free switching in the array level devices in our previous publication[14]. The simulations and nano-sized device results confirm that the composite-W layer supplies not only conventional spin-orbit torque resulting from spin Hall effect but also a damping-like torque induced by spin polarisation along x-direction, enabling the field-free Type-X SOT switching.

Note 2. Type-Y SOT-MRAM architecture considerations.

1. Field-free switching capability:
   Although significant efforts have been made to achieve Type-Z field-free switching, such as the 2019 report by imec demonstrating field-free switching of p-MTJs using the stray field generated by the magnetic hard mask layer[15], we argue that this approach faces significant scalability challenges. Specifically, the magnetic stray field from the hard mask may interfere with neighboring cells in densely packed arrays, leading to crosstalk and operational instability. Moreover, this solution is inherently vulnerable to external magnetic fields. Exposure to such fields could disrupt the delicate balance required for reliable switching, resulting in a high error rate and reduced device performance. These limitations highlight potential drawbacks in implementing this approach for scalable and robust memory technologies.

   In addition to these limitations, the use of a magnetic hard mask layer above the MTJ stack significantly increases the height of the MTJ, leading to high aspect ratio vias required to connect the bottom electrode to the top electrode. These high aspect ratio vias add complexity to the fabrication process, particularly in terms of metal filling and ensuring reliable interconnects. These challenges collectively highlight the drawbacks of this approach for scalable and robust memory technologies[16].

   Another example of field-free switching is the STT-assisted SOT-MRAM design[17-20]. While this approach may be more fabrication-friendly, it introduces significant reliability concerns. Specifically, the requirement for STT current to pass through the MTJ undermines one of the key advantages of SOT-MRAM, which is the separation of the read and write paths. Additionally, the need for precise synchronization between the STT and SOT pulses complicates the control circuitry, necessitating larger peripheral components. This results in an increased device footprint, making STT-assisted SOT-MRAM a less economical solution for embedded memory applications compared to pure SOT-MRAM designs.

   Recently, field-free perpendicular magnetisation switching has also been demonstrated by utilizing the unconventional spin Hall effect (out-of-plane spin) in low crystal symmetry materials with strong spin-orbit coupling[21-25]. While these developments are exciting and reveal intriguing material behaviors, their back-end-of-line (BEOL) and proper MTJ (MR > 100%) integration compatibility are still under active investigation, which poses a significant challenge for practical implementation.

2. Density:
   Cell size, or density (# of device/unit area), is a critical figure of merit for any device in semiconductor manufacturing. In the 2T1M (2 transistors and 1 MTJ) design, we compare three different types of SOT-MRAM (Type-Y, Type-X, and Type-Z) as shown in **S9**, using the 7-nm Fin-FET process design kit[26]. The fin pitch (F) at the 7-nm node is 27 nm[27].

   Within the 2T1M framework, the critical dimension (CD) of the MTJ is limited to 4/3 F,

based on a highly scaled design where the SOC (spin-orbit coupling) layer is placed at the M2-M3 interconnect layers. At these layers, the metal pitch increases by a factor of 1/3 relative to the fin pitch. However, if the MTJ and SOC layer are positioned at higher interconnect layers, the metal pitch increases further (e.g., M4-M5: 1.78 F, M6-M7: 2.36F).

Under these scaling constraints, transitioning from a Type-Y design (4F×8F) to a Type-Z design (3F×8F) offers minimal density improvement while introducing significant engineering challenges. These include the lack of a field-free switching solution, magnetic immunity concerns, and thermal stability issues.

Consequently, while Type-Z may appear advantageous on paper, its practical implementation requires overcoming these substantial hurdles. It is worthy of mention, our composite-W layer can offer conventional spin to enable field-free Type-X switching, which occupies the same foot print as Type-Z SOT-MRAM.

3. Thermal stability:

To achieve stable perpendicular magnetic anisotropy (PMA) in an MTJ, the MgO/CoFeB heterostructure is the preferred combination due to its high interfacial anisotropy energy (K_i). By scaling down the thickness of the ferromagnetic layer, the interfacial anisotropy term can dominate over the shape anisotropy (demagnetizing field). The resulting effective anisotropy (K_{eff}) can be expressed as:

$$K_{eff} = \frac{M_s H_k^{eff}}{2} = K_b + \frac{K_i}{t} - \delta N \frac{M_s^2}{2\mu_0},$$

where $M_s$is the saturation magnetisation, H_k^{eff} is the effective anisotropy field, K_b is the bulk anisotropy (magnetocrystalline), K_i is the interfacial energy, t is the ferromagnetic layer thickness, δN ($N_x + N_y + N_z = 1$, and $\delta N = N_z + N_x$) is the shape anisotropy coefficient, and μ_0 is the permeability of vacuum. And the corresponding thermal stability (Δ) for p-MTJ is:

$$\Delta_{PMA} = \frac{E}{k_B T} = \frac{K_{eff}}{k_B T} \times \frac{t\pi D^2}{4},$$

where D the is diameter of the ferromagnetic layer (critical dimension of p-MTJ), k_B is the Boltzmann constant, T and is the temperature[28,29].

Based on this background, the process window for achieving stable PMA can be estimated for a given interfacial anisotropy energy. As shown in **S10**, for an advanced 3-nm node with F = 45 nm[30,31], a moderate thermal stability ($\Delta < 100$, for low-power application since the switching current is proportional to the thermal stability[32]), reasonable K_i, and M_s, the thickness window for the ferromagnetic layer is very limited to maintain the PMA.

This narrow process window introduces potential yield challenges in the fabrication process. Variations in key parameters, such as ferromagnetic layer thickness and

interfacial anisotropy energy, can arise due to fluctuations in interface quality and crystallinity, which are critical for ensuring consistent PMA across devices. Addressing these challenges is vital for p-MTJ-based technologies.

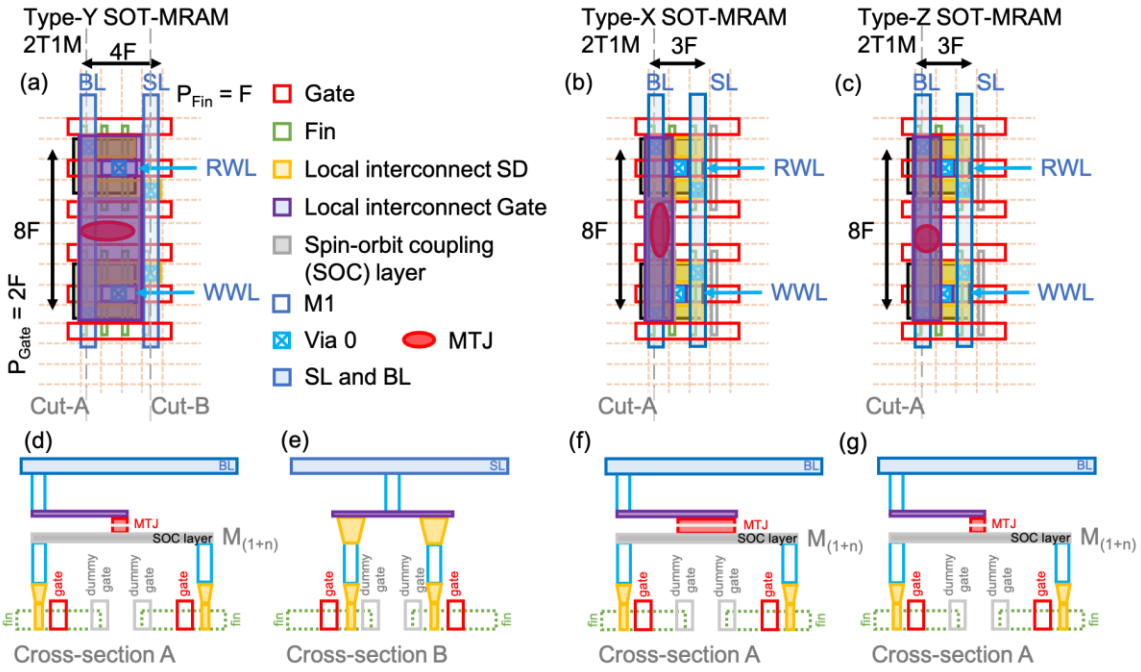
On the other hand, for in-plane MTJs, the thermal stability of Type-Y does not depend on interfacial quality but rather on shape anisotropy, typically characterized by an aspect ratio of 3. This thermal stability can be expressed as:

$$\Delta_{IMA} = \frac{E}{k_B T} = \frac{K_U V}{k_B T} = \frac{M_s H_k V}{2 k_B T},$$

where H_k is the in-plane anisotropy field generated by the shape anisotropy of the ferromagnet. To estimate the thermal stability of Type-Y MTJs, we used OOMMF (Object Oriented MicroMagnetic Framework) to perform micromagnetic simulation to model the in-plane anisotropy field (H_k) as a function of different thickness and critical dimension as shown in **S11**.

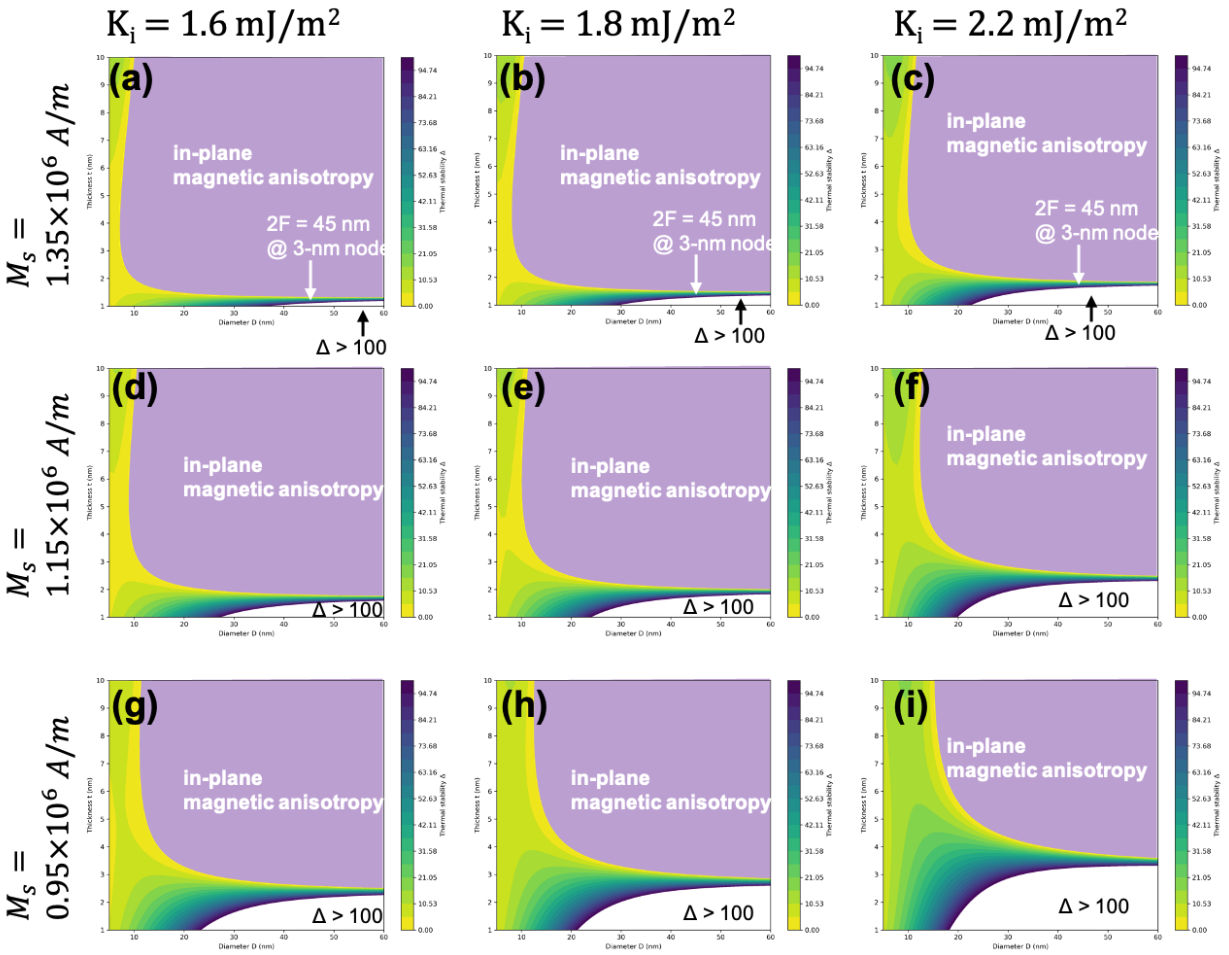
As shown in **S10**, we consider an extreme case where the critical dimension is 45 nm (equivalent to two fin pitches at the 3-nm node). In this scenario, the process window for Type-Y MTJs is significantly broader compared to the case of p-MTJs depicted in **S11**. We note that one can further increase the thermal stability of in-plane MTJ by introducing the bulk magnetic anisotropy (magnetocrystalline) as shown in **S11c**.

This observation highlights the robustness of Type-Y MTJs in terms of manufacturability, particularly in advanced node processes where critical dimensions are further scaled.

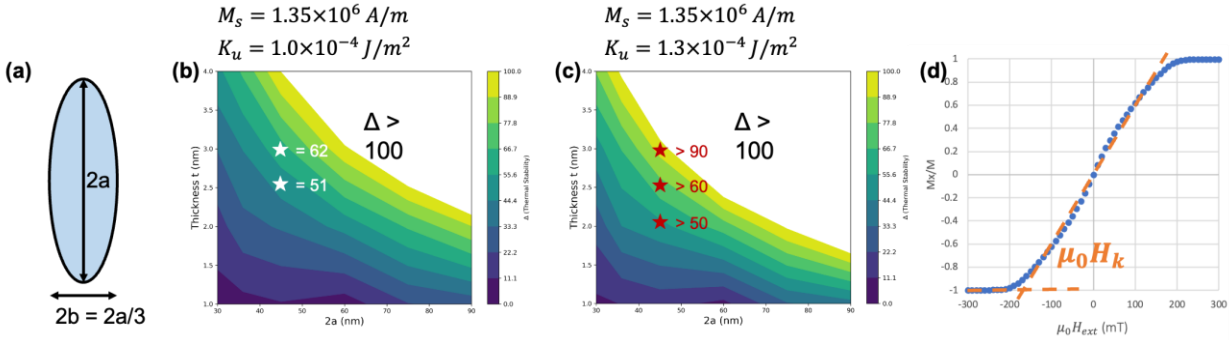


S9 Schematics and layouts of three different types of SOT-MRAM. (a) Top-view schematic of Type-Y 2T1M memory bit-cells with cuts A and B indicated. (b) and (c) Top-view schematics of Type-X and Type-Z 2T1M memory bit-cells, respectively, each with an

indicated line cut. (d) and (e) Cross-sectional views corresponding to cuts A and B in (a), illustrating the integration of the magnetic tunnel junction, spin–orbit coupling layer, and interconnects. (f) and (g) Cross-sectional views corresponding to the line cuts in (b) and (c), respectively.



S10 Thermal stability estimation with different interfacial energy and saturation magnetization of free layer. Each row corresponds to a different saturation magnetization, M_s: (a–c) 1.35 MA/m, (d–f) 1.15 MA/m, and (g–i) 0.95 MA/m. Each column corresponds to a different interfacial energy, K_i. The purple region indicates the free layer with in-plane magnetic anisotropy, while the white region denotes thermal stability values greater than 100, which are not favorable for high-speed and low-power device operation.



S11 Thermal stability estimation of in-plane MTJ. (a) Schematic illustrating the elliptical free layer with in-plane magnetisation used in the thermal stability simulations (major axis = 2 a, AR = 3). (b), (c) Color maps of the simulated in-plane anisotropy field (H_k) under varying magnetic parameters; the stars mark 2a = 45 nm with various targeted thermal stabilities. (d) Resulting H_k values extracted from the simulated M-H loop.

4. Energy efficiency.
   Finally, from the perspective of switching current, Type-Z SOT-MRAM is not the most ideal option. Switching efficiency is a critical parameter in evaluating SOT-MRAM performance as it directly impacts power consumption, speed, and scalability. This efficiency is fundamentally governed by the interplay between the spin-orbit torque (SOT) generated in the spin-orbit coupling (SOC) layer and the thermal stability of the ferromagnetic layer. The switching current density (J_C) for Type-Z (and similarly Type-X) SOT-MRAM can be expressed as:

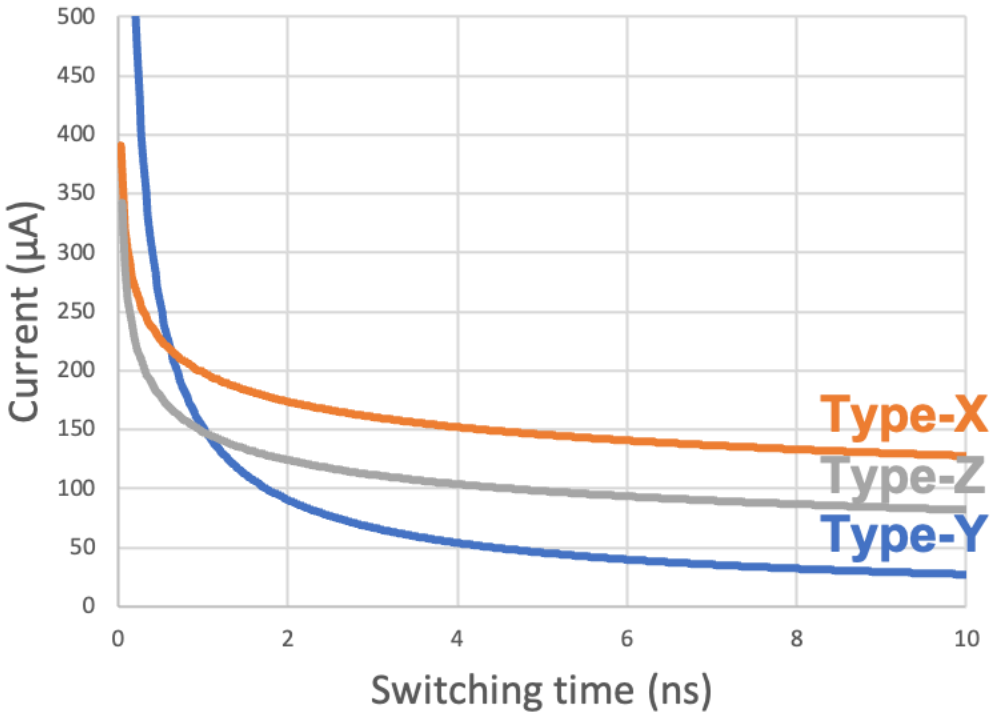
$$J_C = \frac{2e}{\hbar}\frac{M_s t}{\theta}\left(\frac{H_k^{eff}}{2} - \frac{H_x}{\sqrt{2}}\right),$$

   where $\hbar$ is the reduced Plank constant, θ is the spin Hall angle, H_k^{eff} is the effective anisotropy field, and H_x (H_z for Type-X)is the applied in-plane field in parallel to the applied current direction to break the symmetry and enable the deterministic switching[33,34].
   On the other hand, the critical switching current density for Type-Y SOT-MRAM can be expressed as:

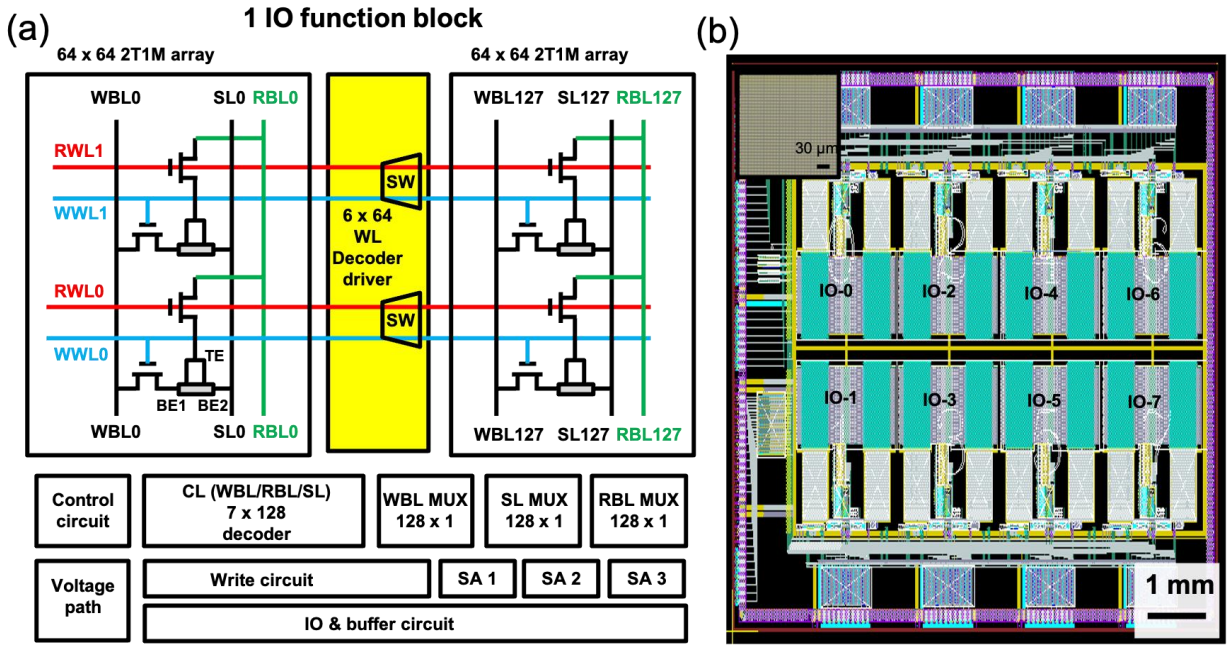
$$J_C = \frac{2e}{\hbar}\frac{\alpha M_s t}{\theta}\left(H_{k,in}^{eff} + \frac{H_{k,out}^{eff}}{2}\right),$$

   where is the α Gilbert damping constant, $H_{k,in}^{eff}$ is the in-plane effective anisotropy field, and $H_{k,out}^{eff}$ is the out-of-plane effective anisotropy fields. Comparing the equations, Type-Y switching is inherently slower due to the precession process. However, the damping constant in the switching current density formula of Type-Y also highlights the potential to reduce switching current, as our experimental results indicate a low damping constant ($\alpha = 0.008 - 0.007$). Furthermore, Type-Y switching is more energy-efficient due to its ability to configure spin polarization to be either parallel or antiparallel to the ferromagnetic layer, as demonstrated by S. Fukami et al. from Prof. Ohno's group[35]. These findings have also been corroborated by micromagnetic simulations from Y. T. Liu et al.[36].

To further validate this concept, we performed additional micromagnetic simulations using OOMMF. For these simulations, we used a thermal stability factor of 50 and investigated the three SOT-switching geometries (Type-X, Type-Y, and Type-Z). For Type-X and Type-Z, external out-of-plane and in-plane fields of 10 mT were applied, respectively. As shown in **S12**, Type-Y switching consumes less current when the switching time exceeds approximately 1 ns.



S12 Comparison of switching speed of Type-X, -Y, and -Z by micromagnetic simulations. Simulated current versus switching time characteristics for three SOT-MRAM device geometries: Type-X, Type-Y, and Type-Z. The plot illustrates the trade-off between switching speed and current consumption, showing that Type-Y offers the lowest switching current in the longer time regime (≥1 ns), highlighting its superior energy efficiency.



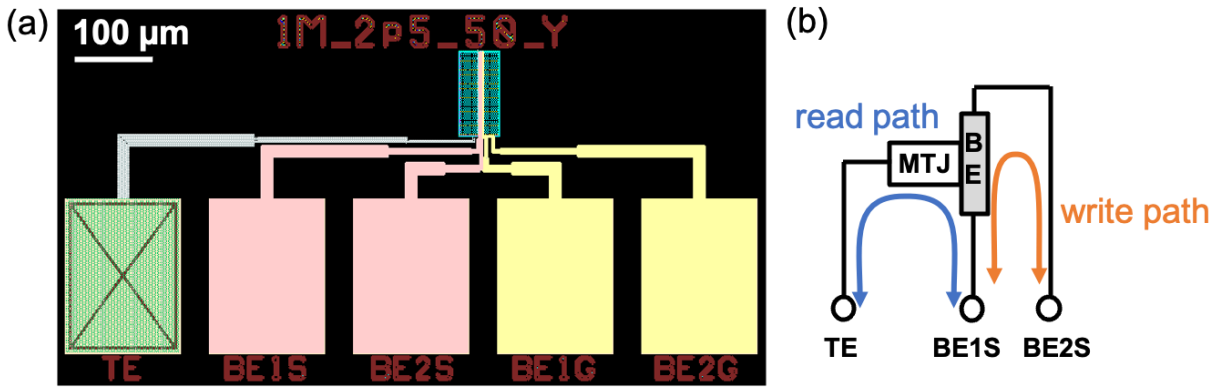
S13. 64-kb SOT-MRAM array layout. (a) IO function block diagram. Each IO function block contains 2 sets of SOT-MRAM arrays containing 64 x 64 bit-cells. (b) Full-chip layout of the 64-kb SOT-MRAM. The inset shows an optical image of the top electrode of the MTJ prior to the deposition of subsequent interconnect layers.

S13a represents the memory access mechanism in 64-kb SOT-MRAM architecture, showing how the word-line (WL) decoder and driver interact with read-word-line (RWL) and write-word-line (WWL) to enable efficient memory operations.

In this array, there are 2^6 set of rows, called read-word-line and write-word-line (WWL), and 2^6 set of columns, called read-bit-line (RBL) and write-bit-line (WBL), and the total number of memory bit-cells in this array is $2^6 \times 2^6$. In addition, there are 2^6 source-line (SL) for routing write current of SOT-MRAM bit-cell. The column lines are fed into the corresponding multiplexers (MUX) and sense amplifier (SA).

Read operation: The read operation is performed by activating the RWL of a target bit-cell with a corresponding "off" WWL. This connects the RBL to the bit-cell MTJ and the heavy metal layer.

Write operation: The write operation is performed by activating the WWL a target bit-cell with a corresponding "off" RWL. This connects the WBL to the heavy metal layer of selected memory bit-cell.



S14. SOT test kit for magnetoresistance characterisation. (a) Layout of the SOT switching test structure designed for magnetoresistance characterisation of three-terminal MTJs. (b) Metal routing configuration illustrating the electrical access points, including the top electrode (TE) and four bottom electrodes (BE1S, BE2S, BE1G, BE2G), which enable direct and independent probing of the MTJ stack. BE1S and BE2S connect to the composite-W spin Hall channel to provide the current path for SOT-induced switching (highlighted in orange double arrow curve). BE1G and BE2G serve as ground electrodes, establishing a defined potential reference for the write path. For magnetoresistance readout, the resistance is typically measured between BE1S and TE (highlighted in blue double arrow curve). The dimensions of the MTJ are described in the Methods section.

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